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1. SCOPE

1.1 Content. This document describes the requirements for linear monolithic microcircuits which are pulse width modulators, adjustable voltage regulators, and MOSFET drivers. The requirements provide a level of microcircuit quality and reliability assurance for acquisition of microcircuits for JPL Mission Class A and B applications.

1.2 Device Type. The device type shall identify the circuit function as follows:

<u>JPL Drawing Number</u>	<u>Generic</u>	<u>Description</u>
CS515570-1,2,3	SG1526B	Regulating Pulse Width Modulator
CS515570-4,5	SG1524B	Regulating Pulse Width Modulator
CS515570-6,7	SG1846	Current Mode PWM Controller
CS515570-8	SG1532	Precision Positive Adjustable Voltage Regulator
CS515570-9, 10	SG1644	Dual High Speed MOSFET Driver
CS515570-11	SG1842	Current Mode PWM Controller

1.2.1 Case Outline. The case outline shall be as shown in MIL-M-38510, Appendix C and as follows:

<u>JPL Drawing Number</u>	<u>Case Description</u>
a. CS515570-1	GDIP1-T18, Configuration A (D-6 18 lead dual-in-line ceramic package)
b. CS515570-2	GDFP1-F24, Configuration A (F-16, 24-lead ceramic, flat pack package; F-8, configuration C, a 24-lead ceramic, flat pack package has been inactive for new design since 29 November 1986, per MIL-M-38510 Rev. H Appendix C Table C-1, Note 15.)
c. CS515570-3	GDFP1-F20, Configuration A (F-9, 20-lead ceramic flat pack); this configuration is not recommended because of potentially higher costs and schedule slippages associated with it.
d. CS515570-4	GDIP1-T16, Configuration A (D-2, 16-lead ceramic, dual-in-line package)
e. CS515570-5	GDFP2-F16, Configuration A (F-5, 16-lead ceramic, flat pack)
f. CS515570-6	GDIP1-T16, Configuration A (D-2, 16-lead ceramic, dual-in-line package)

- g. CS515570-7 GDFP2-F16, Configuration A (F-5, 16-lead ceramic, flat pack)
- h. CS515570-8 GDFP1-F14, Configuration A (F-2, 14-lead ceramic flat pack, glass-sealed)
- i. CS515570-9 GDIP1-T14, Configuration A (D-1, 14-lead, ceramic, dual-in-line package)
- j. CS515570-10, 11 GDFP1-F10, Configuration A (F-4, 10 lead, ceramic, flat pack)

1.3 Manufacturer's Maximum Ratings. The following data are for design information only.

	Parameter	Rating
a. Input Voltage (V_{IN})	SG1526B, SG1846, SG1524B	40V 42V
b. Collector Voltage (V_C)	SG1526B, SG1846 SG1524B	40V 60V
c. Logic Input(s) Voltage	SG1526B, SG1524B, SG1846 SG1644	-0.3 to 5.5V 7V
d. Analog Input(s) Voltage	SG1526B, SG1524B, SG1846 pin 2, pin 3 SG1842	-0.3 to V_{IN} -0.3 TO 6.3V
e. Source/Sink Load Current (each Output)	SG1526B, SG1524B, SG1846	200mA
f. Reference Load Current	SG1526B, SG1524B SG1846 SG1532	50mA 30mA 25mA
g. Logic Sink Current	SG1526B	15mA
h. Oscillator Charging Current	SG1524B, SG1846	5mA
i. Operating Junction Temperature	SG1526B, SG1524B, SG1846, SG1532, SG1644, SG1842	150°C
j. Storage Temperature Range	SG1526B, SG1524B, SG1846, SG1532, SG1644, SG1842	-65 to 150°C

k.	Lead Temperature (Soldering, 10 seconds)	SG1526B, SG1524B, SG1846, SG1532, SG1644, SG1842	300°C
l.	Supply Voltage	SG1644 SG1842	22V 30V
m.	Source/Sink Output Current Continuous Pulse, 500 ns	SG1644	±0.5A ±3.0A
n.	Input voltage from V _{IN} to V ₋ Continuous Pulse	SG1532	40V 50V
o.	V _{IN} to V _{OUT} Differential	SG1532	40V
p.	Output Current Continuous	SG1532 SG1842	250 mA 350 mA
	Peak	SG1842	±1A
q.	Current from V _Z	SG1532	100 mA
r.	Error Amp Output Sink Current (pin 1, comp)	SG1842	10 mA
s.	Output Energy (Capacitive Load)	SG1842	5 microjoules

1.4 Manufacturer's Recommended Operating Conditions.

	Parameter	Rating	
a.	Input Voltage Supply Voltage Range Input Voltage Range Supply Voltage Supply Voltage	SG1526B SG1524B SG1846 SG1532 SG1644 SG1842	8 to 35V 7 to 40V 8 to 40V 5V to 45V 4.5V to 20V 30V
b.	Collector Voltage	SG1526B SG1524B SG1846	4.5 to 35V 0 to 60V 4.5 to 40V
c.	Sink/Source Load Current (each Output)	SG1526B, SG1524B, SG1846	0 to 100mA
d.	Reference Load Current	SG1526B, SG1524B SG1846 SG1532	0 to 20mA 0 to 10mA 5mA
e.	Error Amplifier Common Mode Range	SG1524B	2.3V to V _{REF}

f.	Current Limit Sense Common Mode Range	SG1524B	0V to V_{IN} -2.5V
g.	Oscillator Frequency Range	SG1526B, SG1846 SG1524B SG1842	1Hz to 500KHz 100Hz to 400KHz 100Hz to 500KHz
h.	Oscillator Timing Resistor	SG1526B, SG1524B SG1846 SG1842	2Kohm to 150Kohm 2Kohm to 100Kohm 520ohm to 150Kohm
i.	Oscillator Timing Capacitor	SG1526B SG1524B, SG1846 SG1842	470pF to 20uF 1nF to 0.1μF
j.	Oscillator Charging Current	SG1524B	1000pF to 1μF
k.	Available Dead-time Range at 40KHz	SG1526B	25μA to 1.8mA 5 to 50%
l.	Operating Ambient Temperature Range	SG1526B, SG1524B, SG1846, SG1532, SG1644, SG1842	-55°C to 125°C
m.	Output Current Range	SG1532 SG1842	1mA to 100mA ±1A Peak 200mA Continuous
n.	Zener Current	SG1532	20 mA
o.	Frequency Range	SG1644	DC to 1.5 MHz
p.	Peak Pulse Current	SG1644	±3A
q.	Logic Input Voltage	SG1644	-0.5V to 5.5V
r.	Output Voltage Range	SG1532	2.0V to 38V
s.	Error Amp Output Sink Current (pin 1, comp)	SG1842	5mA

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents. The following documents, of the issue in effect on date of invitation of bids or request for proposal form a part of this specification to the extent specified herein.

SPECIFICATION

Military

MIL-M-38510/102B Microcircuits, Linear, Voltage Regulator, Monolithic Silicon.

MIL-M-38510/126B Microcircuits, Linear, Regulating, Pulse-Width Modulator, Monolithic Silicon.

MIL-M-38510/702 Microcircuits, Linear, Regulating, Pulse-Width Modulators, Monolithic Silicon.

STANDARD

Military

MIL-STD-883 Test Methods and Procedures for
Microelectronics.

2.2 Precedence. In the event of conflict between the text of this document and the documents referenced herein, the text of this document shall take precedence.

3. REQUIREMENTS

3.1 Item Requirements. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. The manufacturer shall notify JPL of changes in product design or masks.

3.2 Design, Construction and Physical Dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal Connections. The terminal connections shall be as specified herein.

3.2.2 Block Diagram. The block diagrams shall be as shown herein.

3.2.3 Case Outlines. The case outlines shall be in accordance with paragraph 1.2.1 herein.

3.3 Lead Material and Finish. The lead or terminal material and finish shall be gold plated or solder dipped in accordance with MIL-M-38510.

3.4 Electrical Performance Characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in Table II (SG1526B), III (SG1524B), IV (SG1846), V (SG1842), VII (SG1532) or IX (SG1644) herein as applicable, and apply over the full recommended ambient operating temperature range.

3.5 Electrical Test Requirements. The electrical test requirements shall be the subgroups specified in Table I herein. The electrical tests for each subgroup are described in Table II, III, IV, V, VII or IX as applicable.

3.5.1 Electrical Test Program. A copy of the test program in a readable format and data, taken on a subject device type over temperature, shall be supplied to JPL for review and approval. Only the JPL approved program shall be used for testing.

3.5.2 Radiation Testing. The parts shall be tested per paragraph 4.4.4 herein when specified in the contract or purchase order.

3.5.3 Delta Criteria. The electrical parameters identified in Tables II, III, IV, V, VII and IX herein shall be measured and recorded before and after each burn-in of respective microcircuits. After interim or final electrical parameter measurements, the change (delta) in the respective parameters identified in respective Tables VI, VIII and X shall be calculated between the initial electrical measurement and the present (interim or final) measurement.

3.6 Marking. Devices shall be marked in accordance with MIL-M-38510, except that the military number shall be replaced by the JPL drawing number and vendor part number per 6.5 herein. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the original container.

3.6.1 Serialization. All devices shall be serialized in accordance with MIL-M-38510, Class S quality level.

3.7 Quality Assurance Requirements. Microcircuits furnished in conformance to this specification shall have been subjected to, and passed all the requirements, tests and inspections including screening and quality conformance inspections as detailed in paragraph 4. herein and in the detail specification.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and Inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and MIL-STD-883, Methods 5005 and 5007, as applicable, except as modified herein.

4.1.1 Wafer Lot Acceptance. Devices furnished under this specification shall be from wafer lots that are subjected to and successfully meet the wafer lot acceptance inspections and tests specified in MIL-STD-883, Method 5007.

4.1.2 SEM Requirements. Test slices from each wafer shall be submitted to scanning electron microscope (SEM) analysis in accordance with MIL-STD-883, Method 2018, when wafer metallization is done in sequential wafer subgroups without a unique identifier for each subgroup.

4.1.3 Internal Visual (Precap). Precap inspection shall be in accordance with MIL-STD-883, Method 2010, condition A.

4.2 Screening. Screening shall be in accordance with MIL-STD-883, Method 5004, level S, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply to respective microcircuit types:

- a. Delete the sequence specified in MIL-STD-883, Method 5004, 3.1.9 through 3.1.13, and substitute Table I, lines 1 through 7 herein.
- b. Static Burn-in Test (MIL-STD-883, Method 1015). Static test (test condition B) shall be done using the circuit shown herein or equivalent by JPL approval. Free air ambient temperature (TA) shall be between 125 and 128°C. Test duration shall be 96 hours minimum.

- c. Dynamic Burn-in Test (MIL-STD-883, Method 1015). Dynamic test (test condition D) shall be done using the circuit shown herein or equivalent by JPL approval. Free air ambient temperature (TA) shall be between 125 and 128°C. Test duration shall be 240 hours minimum.
- d. Pre-burn-in, interim and final electrical parameters measurements shall be done for the respective microcircuits specified in Table II, III, IV, V, VII or IX herein.

4.2.1 Percent Defective Allowable (PDA).

- a. The PDA for each inspection lot or subplot submitted to burn-in and interim electrical parameters shall be five percent (or one device, whichever is greater) cumulative across all burn-ins on all parametric failures. The PDA on functional failures shall be three percent or one device, whichever is greater.
- b. The verified failures, excluding devices which fail only the delta limits, divided by the total number of devices in the lot initially submitted to burn-in, shall be used to determine the percent defective for the lot. Unless otherwise specified, lots may be resubmitted only when the observed percent defective does not exceed 15 percent. The PDA for the second submittal is five percent.

4.3 Qualification Inspection. Qualification inspection in accordance with MIL-M-38510 is not required.

4.4 Quality Conformance Inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and MIL-STD-883, Method 5005. Group A and Group B inspections shall be performed on each inspection lot in accordance with MIL-STD-883, Method 5005 (Table I and IIa) or as otherwise specified. Group D (MIL-STD-883, Method 5005 Table IV) shall be performed on a periodic basis as specified in MIL-M-38510. Generic test data may be used to satisfy the requirements of group D inspections. If specified in the purchase order or contract, Group E inspections shall be performed on each inspection lot in accordance with MIL-STD-883, Method 5005 (Table V) or as otherwise specified.

4.4.1 Group A Inspection. Group A inspection shall consist of the test subgroups and Lot Tolerance Percent Defective (LTPD) values shown in MIL-STD-883, Table I, Method 5005, Class S, and as specified in Table I herein.

4.4.2 Group B Inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in MIL-STD-883, Method 5005, Table IIa, Class S, and as follows:

- a. End-point electrical parameters shall be as specified in Table I herein.
- b. Steady state life test (MIL-STD-883, Method 1005) conditions:

- 1) Dynamic test circuit. (Same as the screening dynamic test circuit.)
 - 2) $T_A = +125 \pm 3/-0^\circ\text{C}$.
 - 3) Test duration: 1000 hours minimum. No accelerated life testing shall be permitted.
 - 4) Interim data shall be read and recorded at room temperature at 250 hour, 500 hour, and 750 hour duration.
 - 5) The LTPD shall be five (sample size = 45, 0 rejects allowed).
 - 6) The delta criteria of Tables VI, VIII and X shall be applied to the respective microcircuit's corresponding parameters for the life test.
- c. Electrical reject parts from the lot shall be used for subgroups 1, 2, 3, and 4. Subgroup 7 is waived.

4.4.3 Group D Inspection. Group D inspections shall consist of the test subgroups and LTPD values shown in MIL-STD-883, Method 5005, Table IV, Class S, and the end-point electrical parameters shall be as specified in Table I herein.

4.4.4 Group E Inspection. When specified in the contract or purchase order, Group E inspection shall be in accordance with test procedures specified in MIL-STD-883, Method 5005, Table V. The total dose shall be 100 krad (Si), unless otherwise specified. End-point electrical parameters shall be performed twice. The first measurement shall start within one hour after the end of the irradiation as specified in MIL-STD-883, Method 1019. The second measurement, for rebound (post-irradiation effect) analysis, shall be performed on the entire sample with devices stored for 10 days at room temperature with no bias applied. No rejects are allowed in either set of measurements.

4.4.5 Destructive Physical Analysis (DPA). Destructive physical analysis shall be in accordance with MIL-STD-883, Method 5009 on screened parts. A minimum of three devices or 1% of the inspection lot, whichever is greater, to a maximum of five devices, shall be used. At least one of the devices shall be used for internal water vapor content analysis.

4.5 Data Reporting. A copy of the following data, as applicable, shall be supplied:

- a. Attributes data for all screening tests (see 4.2 herein) and all variables data for all screening burn-ins and steady state life tests (see 3.5 herein), including pre-burn-in, interim and final electrical parameter measurements.
- b. A copy of each radiograph (see Method 5004, 3.1.18).

- c. The quality conformance inspection data (see 4.4 herein), including Groups A, B, D and E parameter measurements.
- d. Delta calculations for all parameters listed in Tables VI, VIII and X herein.
- e. Wafer acceptance test report (see 4.1.1 herein).
- f. Scanning electron microscope (SEM) report (see 4.1.2 herein).
- g. Certificate of compliance to this specification.

4.5.1 Data Report Format. Data shall be identified by part type, lot number and serial number range. The required electrical data and delta analyses shall be presented in easily readable condition, in serial number order, such that all data for a particular temperature is grouped together and in test sequence order. Variables data and delta calculations shall be supplied on a magnetic media in computer readable format, provided the format is approved by the procuring activity.

4.6 Problem Notification. The JPL technical representative shall be notified within twenty-four hours, of the occurrence of the following:

- a. If the number of nonconforming parts exceeds five percent of the lot for any of the respective, applicable tests in Tables II, III, IV, V, VII or IX herein.
- b. Any parts failing Group B, D, or E tests.
- c. Other delays due to test equipment breakdown, test error or testing related problems which adversely affect the schedule.

4.7 Control Units. A control unit is a device identical to the test specimens and from the same lot which is not subjected to any stresses applied to the test specimens, but is used to verify the resolution, accuracy and repeatability of measurement equipment. Three control units shall be read and recorded before and after each read and record operation on the lot.

4.8 JPL Source Inspection. JPL will provide source inspection for preseal visual (to MIL-STD-883, Method 2010, Condition A), preship inspection (to MIL-STD-883, Method 2009), and preship review of the lot data books. The manufacturer shall provide 48 hour notification, unless otherwise specified, prior to parts arriving at the appropriate inspection point and an adequately equipped work station with electrostatic discharge (ESD) protection to perform the inspection.

5. PACKAGING

5.1 Packaging Requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

5.2 Electrostatic Discharge (ESD) Sensitivity. The devices supplied in accordance with this specification shall be considered to be ESD sensitive and

require further protection and shall use one of the packaging requirements in accordance with MIL-M-38510, Paragraph 5, Packaging, Category A.

6. NOTES

6.1 Intended Use. Microcircuits conforming to this specification are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for original equipment manufacturer (OEM) application. When a military specification exists and the product covered by this specification has been qualified for listing on QPL-38510 Class S, this specification shall be inactivated and shall not be used for a new design. The QPL-38510 Class S product shall be the preferred item for all applications. The microcircuits shall be of a quality and reliability assurance level suitable for JPL mission Class A and Class B; both non-repairable, long duration, inter-planetary space craft applications.

6.2 Ordering Data. The contract or purchase order should specify the following:

- a. Vendor part number and JPL drawing number (see 6.5 herein).
- b. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number.
- c. Requirement for inspection notification, if other than 48 hours (see 4.8 herein).
- d. JPL Parts Trace Number.
- e. Requirement for radiation tests and level. (see 3.5.2 herein).
- f. Option to have JPL perform DPA. (See 4.4.5 herein.)

6.3 Handling. Electrostatic sensitive devices must be handled with certain precautions to avoid damage due to electrostatic charge. The following handling practices are recommended:

- a. Devices should be handled on benches with conductive and grounded surfaces.
- b. Provide a ground for test equipment, tools, and operator.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or anti-static carriers.
- e. Avoid use of plastic, rubber, or silk.
- f. Maintain relative humidity above 50 percent, if practical.
- g. Operator should be grounded when handling device.

h. Handlers and other such machinery should be grounded.

6.4 Certificate of Conformance. Certificate of conformance to this specification, signed by an authorized representative of the manufacturer, must accompany each shipment.

6.5 Approved Sources of Supply. The following products and manufacturers are approved by JPL:

Similar to Vendor Part No.	Package	JPL Drawing Number	CAGE Number	Vendor Name and Address
SG1526BJ	DIP (18-lead)	CS515570-1	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1526BF	Flatpack (24-lead)	CS515570-2	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1526BSF	1/ Flat pack (20- lead)	CS515570-3	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1524BJ	DIP (16-lead)	CS515570-4	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1524BF	Flatpack (16-lead)	CS515570-5	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1846J	DIP (16-lead)	CS515570-6	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1846F	Flatpack (16-lead)	CS515570-7	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1532F	Flatpack (14-lead)	CS515570-8	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1644J	DIP (14-lead)	CS515570-9	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1644F	Flatpack (10-lead)	CS515570-10	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641
SG1842	Flatpack (10-lead)	CS515570-11	34333	Silicon General Inc. 11861 Western Ave. Garden Grove, CA 92641

NOTES: 1/ This configuration is not recommended because of potentially higher costs and schedule slippages associated with it.

Table I. Screening and Quality Conformance Inspection Requirements

Line No.	Applicable Tests and MIL-STD-883 Test Methods	Subgroups
1	Pre burn-in electrical parameters (Method 5004)	1, 2, 3, 7, 8, 9, 10, 11
2	Static Burn-in	
3	Interim electrical parameters (Method 5004)	Δ1, 7
4	Dynamic burn-in	
5	Same as line 3	Δ1*, 7
6	Final electrical parameters	1, 2, 3, 7, 8, 9, 10, 11
7	Group A test requirements (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11
8	Group B end-point electrical parameters (Method 5005)	Δ1, 2, 3, 7, 8, 9, 10, 11
9	Group D end-point electrical parameters (Method 5005)	1, 2, 3, 7
10	Group E end-point electrical parameters (Method 5005)**	1, 7

* PDA applies to subgroup 1 and 7 (see 4.2.1)

** When required per paragraph 6.2.e. herein.

Δ Tables VI, VIII and X Delta criteria shall be calculated with reference to the line 1 electrical parameters measurement. For line 8, the delta calculations shall be made with reference to the Subgroup 5 pre-life-test measurements.

Table II. SG1526B Electrical Characteristics
Unless otherwise specified, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and $V_{IN} = 15\text{V}$.

Parameter	Test Conditions	Spec Limit		Units
		Min.	Max.	
Reference Section 1/				
Output Voltage, V_{REF}	$T_J = 25^{\circ}\text{C}$ $V_{IN} = 8$ to 35V $I_L = 0$ to 20mA Over operating T_J	4.95	5.05	V
Line Regulation		10	mV	
Load Regulation		20	mV	
Temperature Stability		50	mV	
/				
Total Output Voltage Range		4.90	5.10	V
Short Circuit Current	$V_{REF} = 0\text{V}$	25	125	mA
Undervoltage Lockout Section				
NOT-RESET Output Voltage	$V_{REF} = 3.8\text{V}$		0.4	V
NOT-RESET Output Voltage	$V_{REF} = 4.8\text{V}$	2.4		V
Oscillator Section 2/				
Initial Accuracy	$T_J = 25^{\circ}\text{C}$		± 8	%
Voltage Stability	$V_{IN} = 8$ to 35V		1.0	%
Temperature Stability	Over operating T_J		10	%
/				
Minimum Frequency	$R_T = 150\text{Kohms}, C_T = 20\mu\text{F}$		1.0	Hz
Maximum Frequency	$R_T = 2\text{Kohms}, C_T = 470\text{pF}$	500		KHz
Sawtooth Peak Voltage	$V_{IN} = 35\text{V}$	2.5	3.5	V
Sawtooth Valley Voltage	$V_{IN} = 8\text{V}$	0.5	1.1	V
NOT-SYNC Pulse Width	$R_L = 2.0\text{Kohms}$ to V_{REF}		2	μs
Error Amplifier Section 3/				
Input Offset Voltage, V_{IO}	$R_S \leq 2\text{Kohms}$		5	mV
Input Bias Current, I_{IB}			-1,000	nA
Input Offset Current, I_{IO}			100	nA
DC Open Loop Gain	$R_L \geq 10\text{Mohms}$	64		dB
High Output Voltage	$V_{PIN1} - V_{PIN2} \geq 150\text{mV}$, $I_{SOURCE} = 100\mu\text{A}$	3.6		V
Low Output Voltage	$V_{PIN2} - V_{PIN1} \geq 150\text{mV}$, $I_{SINK} = 100\mu\text{A}$		0.4	V
Common Mode Rejection	$R_S \leq 2\text{Kohms}$	70		dB
Supply Voltage	$V_{IN} = 8\text{V}$ to 35V	66		dB
Rejection				
PWM Comparator Section 2/				
Minimum Duty Cycle	$V_{COMPENSATION} = 0.4\text{V}$		0	%
Maximum Duty Cycle	$V_{COMPENSATION} = 3.6\text{V}$	45		%
Digital Ports (NOT-SYNC, NOT-SHUTDOWN, and NOT-RESET)				
HIGH Output Voltage	$I_{SOURCE} = 40\mu\text{A}$	2.4		V
LOW Output Voltage	$I_{SINK} = 3.6\text{mA}$		0.4	V
HIGH Input Current, I_{IH}	$V_{IH} = 2.4\text{V}$		-200	μA

LOW Input Current, I_{IL} NOT-SHUTDOWN Delay to Output	$V_{IL} = 0.4V$ 7/		-360 200	μA ns
Current Limit Comparator Section 4/				
Sense Voltage	$R_s \leq 50$ ohms	90	110	mV
Input Bias Current			-10	μA
Delay to Output 7/			400	ns
Soft-Start Section				
Error Clamp Voltage	NOT-RESET = 0.4V		0.4	V
C_s Charging Current	NOT-RESET = 2.4V	50	150	μA
Output Drivers (each output) 5/				
HIGH Output Voltage	$I_{SOURCE}=20mA$ $I_{SOURCE}=100mA$	12.5 12		V
LOW Output Voltage	$I_{SINK}=20mA$ $I_{SINK}=100mA$		0.3 2	V
Collector Leakage	$V_c=40V$		150	μA
Rise Time	$C_L=1000pF$		0.4	μs
Fall Time	$C_L=1000pF$. 0.15	μs
Power Consumption Section 6/				
Standby Current	NOT-SHUTDOWN=0.4V		30	mA

NOTES:

- 1/ $I_L = 0$ mA
- 2/ $F_{OSC} = 40KHz$ ($R_T = 4.12$ Kohm $\pm 1\%$, $C_T = 0.01\mu F$, $R_D = 0$ ohm)
- 3/ $V_{CM} = 0$ to 5.2V
- 4/ $V_{CM} = 0$ to 12V
- 5/ $V_c = 15V$
- 6/ $V_{IN} = 35V$
- 7/ These parameters are guaranteed over the recommended operating conditions.

Table III. SG1524B Electrical Characteristics
 Unless otherwise specified, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and $+V_{IN} = 20\text{V}$

Parameter	Test Conditions	Spec. Limit		Units
		Min.	Max.	
Reference Section 1/				
Output Voltage, V_{REF}	$T_J = 25^{\circ}\text{C}$	4.95	5.05	V
Line Regulation	$V_{IN} = 7\text{V}$ to 40V		20	mV
Load Regulation	$I_L = 0$ to 20 mA		30	mV
Temperature Stability 5/	Over Operating Temperature Range		50	mV
Total Output Voltage Range	Over Line, Load and Temperature	4.90	5.10	V
Short Circuit Current	$V_{REF} = 0\text{V}$	25	120	mA
Undervoltage Lockout Section				
Threshold Voltage		4.3	4.7	V
Oscillator Section 2/				
Initial Accuracy	$T_J = 25^{\circ}\text{C}$	42	48	KHz
Voltage Stability	$V_{IN} = 7\text{V}$ to 40V		1	%
Temperature Stability 5/	Over Operating Range		2	%
Minimum Frequency	$R_T = 150\text{Kohms}$, $C_T = 0.1\mu\text{F}$		140	Hz
Maximum Frequency	$R_T = 2\text{Kohms}$, $C_T = 470\text{pF}$	400		KHz
Sawtooth Peak Voltage	$V_{IN} = 40\text{V}$		3.9	V
Sawtooth Valley Voltage	$V_{IN} = 7\text{V}$	0.6		V
Clock Amplitude			3.0	V
Clock Pulse Width		0.2	1.2	μs
Error Amplifier Section 3/				
Input Offset Voltage, V_{IO}	$R_S \leq 2\text{Kohms}$		5	mV
Input Bias Current, I_{IB}			5	μA
Input Offset Current, I_{IO}			1	μA
DC Open Loop Gain	$R_L \geq 10\text{Mohms}$	60		dB
Output Low Level	$I_{SINK} = 100\mu\text{A}$; $V_{PIN2} - V_{PIN1} \geq 150\text{mV}$		0.5	V
Output High Level	$I_{SOURCE} = 100\mu\text{A}$; $V_{PIN2} - V_{PIN1} \geq 150\text{mV}$	3.8		V
Common Mode Rejection	$V_{CM} = 2.3\text{V}$ to V_{REF}	70		dB
Supply Voltage Rejection	$V_{IN} = 7\text{V}$ to 40V	76		dB
Gain-Bandwidth Product 5/	$T_J = 25^{\circ}\text{C}$	1		MHz
P.W.M. Comparator 2/				
Minimum Duty Cycle	$V_{COMP} = 0.5\text{V}$		0	%
Maximum Duty Cycle	$V_{COMP} = 3.9\text{V}$	45		%
Current Limit Amplifier Section 4/				
Sense Voltage		180	220	mV
Input Bias Current			-10	μA
Shutdown Input Section				
HIGH Input Voltage		2.0		V
HIGH Input Current	$V_{SHUTDOWN} = 5.0\text{V}$		1	mA
LOW Input Voltage			0.6	V

Output Section (each transistor)				
Collector Leakage Current	$V_{CE} = 60V$		50	μA
Collector Saturation Voltage	$I_C = 10mA$ $I_C = 100mA$		0.4 2.0	V V
Emitter Output Voltage	$I_E = 10mA$ $I_E = 100mA$	17.5 17		V V
Emitter Voltage Rise Time 5/	$R_E=2Kohms, T_A=25^\circ C$		0.5	μs
Collector Voltage Fall Time	$R_C=2Kohms, T_A=25^\circ C$		0.2	μs
Power Consumption				
Standby Current	$V_{IN}=40V, V_{SHUTDOWN}=2.0V$		12	mA

NOTES: 1/ $I_L = 0mA$ 2/ $F_{OSC}=43KHz$ ($R_T=2700$ ohms, $C_T=0.01\mu F$)3/ $V_{CM}= 2.3V$ to V_{REF} 4/ $V_{CM}= 0V$ to $17.5V$

5/ These parameters are guaranteed over the recommended operating conditions.

Table IV. SG1846 Electrical Characteristics
Unless otherwise specified, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and $+V_{IN}=15\text{V}$

Parameter	Test Conditions	Spec. Limit		Units
		Min.	Max.	
Reference Section				
Output Voltage, V_{REF}	$T_J = 25^{\circ}\text{C}$, $I_o = 1\text{mA}$	5.05	5.15	V
Line Regulation	$V_{IN} = 8\text{V}$ to 40V		20	mV
Load Regulation	$I_L = 1\text{mA}$ to 10mA		15	mV
Temperature Stability 1/			TBD	mV/ $^{\circ}\text{C}$
Total Output Variation 1/	Line, Load and Temperature	5.00	5.20	V
Output Noise Voltage 1/	$10\text{Hz} \leq f \leq 10\text{KHz}$, $T_J = 25^{\circ}\text{C}$		TBD	uV
Long Term Stability 1/	$T_J = 125^{\circ}\text{C}$, 1000Hrs.		TBD	mV
Short Circuit Output Current	$V_{REF} = 0\text{V}$	-10		mA
Oscillator Section 6/				
Initial Accuracy	$T_J = 25^{\circ}\text{C}$	39	47	KHz
Voltage Stability	$V_{IN} = 8\text{V}$ to 40V		2	%
Temperature Stability 1/	Over Operating Range		TBD	%
Sync Output High Level		3.9		V
Sync Output Low Level			2.5	V
Sync Input High Level	Pin 8 = 0V	3.9		V
Sync Input Low Level	Pin 8 = 0V		2.5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V		1.5	mA
Error Amp Section				
Input Offset Voltage, V_{IO}			5	mV
Input Bias Current, I_{IB}			-1	μA
Input Offset Current, I_{IO}			250	nA
Common Mode Range	$V_{IN} = 8\text{V}$ to 40V	0	$V_{IN}-2\text{V}$	V
Open Loop Voltage Gain	$V_o = 1.2\text{V}$ to 3V , $V_{CM} = 2\text{V}$	80		dB
Unity Gain Bandwidth 1/	$T_J = 25^{\circ}\text{C}$	0.7		MHz
CMRR	$V_{CM} = 0\text{V}$ to 38V , $V_{IN} = 40\text{V}$	75		dB
PSRR	$V_{IN} = 8\text{V}$ to 40V	80		dB
Output Sink Current	$V_{ID} = -15\text{mV}$ to -5V , $V_{PIN7} = 1.2\text{V}$	2		mA
Output Source Current	$V_{ID} = 15\text{mV}$ to 5V , $V_{PIN7} = 2.5\text{V}$	-0.4		mA
High Level Output Voltage	$R_L = 15\text{K ohms}$ (Pin 7)	4.3		V
Low Level Output Voltage	$R_L = 15\text{K ohms}$ (Pin 7)		1	V
Current Sense Amplifier Section				
Amplifier Gain 2/ 3/	$V_{PIN3} = 0\text{V}$, Pin 1 Open	2.5	3.0	V

Maximum Differential Input Signal ($V_{PIN4}-V_{PIN3}$)	Pin 1 Open $R_L=15K$ ohms (Pin 7)	1.1		V
<u>2/ 3/</u> Input Offset Voltage <u>2/</u>	$V_{PIN1} = 0.5V$, Pin 7 Open		25	mV
CMRR	$V_{CM} = 1V$ to $12V$	60		dB
PSRR	$V_{IN} = 8V$ to $40V$	60		dB
Input Bias Current <u>2/</u>	$V_{PIN1} = 0.5V$, Pin 7 Open		-10	μA
Input Offset Current <u>2/</u>	$V_{PIN1} = 0.5V$, Pin 7 Open		1	μA
Input Common Mode Range		0	$V_{IN}-3$	V
Delay to Outputs <u>1/</u>	$T_J = 25^\circ C$		500	ns
Current Limit Adjust Section				
Current Limit Offset Voltage <u>2/</u>	$V_{PIN3} = 0V$, $V_{PIN4}=0V$, Pin 7 Open	0.45	0.55	V
Input Bias Current	$V_{PIN5} = V_{REF}$, $V_{PIN6} = 0V$		-30	μA
Shutdown Terminal Section				
Threshold Voltage		250	400	mV
Input Voltage Range		0	V_{IN}	V
Minimum Latching Current (I_{PIN1}) <u>4/</u>		3.0		mA
Maximum Non-Latching Current (I_{PIN1}) <u>5/</u>			0.8	mA
Delay to Outputs <u>1/</u>	$T_J = 25^\circ C$		600	ns
Output Section				
Collector Emitter Voltage		40		V
Collector Leakage Current	$V_C = 40V$		200	μA
Output Low Level	$I_{SINK} = 20mA$ $I_{SINK} = 100mA$		0.4 2.1	V V
Output High Level	$I_{SOURCE} = 20mA$ $I_{SOURCE} = 100mA$	13 12		V V
Rise Time <u>1/</u>	$C_L=1nF$, $T_J=25^\circ C$		300	ns
Fall Time <u>1/</u>	$C_L=1nF$, $T_J=25^\circ C$		300	ns
Under-Voltage Lockout Section				
Start-Up Threshold			8.0	V
Threshold Hysteresis			TBD	V
Total Standby Current				
Supply Current			21	mA

NOTES:

1/ These parameters are guaranteed over the recommended operating conditions.

2/ Parameter measured at trip point of latch with $V_{PIN5} = V_{REF}$, $V_{PIN6} = 0V$.

3/ Amplifier gain defined as: $G = (\Delta V_{PIN7}) / (\Delta V_{PIN4})$; $V_{PIN4} = 0V$ to $1.0V$

4/ Current into Pin 1 guaranteed to latch circuit in shutdown state.

5/ Current into Pin 1 guaranteed not to latch circuit in shutdown state.

6/ $R_T = 10K$ ohms, $C_T = 4.7nF$

Table V. SG1842 Electrical Characteristics
Unless otherwise specified, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and $+V_{IN}=15\text{V}$

Parameter	Test Conditions	Spec. Limit		Units
		Min.	Max.	
Reference Section				
Output Voltage, V_{REF}	$T_J = 25^{\circ}\text{C}$, $I_o = 1\text{mA}$	4.95	5.05	V
Line Regulation	$V_{IN} = 12\text{V}$ to 25V		20	mV
Load Regulation	$I_L = 1\text{mA}$ to 20mA		25	mV
Temperature Stability 1/ Total Output Variation 1/ Output Noise Voltage 1/	Line, Load and Temperature $10\text{Hz} \leq f \leq 10\text{KHz}$, $T_J=25^{\circ}\text{C}$	4.90	.4 5.10	mV/ $^{\circ}\text{C}$ V uV
Long Term Stability 1/ Short Circuit Output Current	$T_J=125^{\circ}\text{C}$, 1000Hrs. $V_{REF}=0\text{V}$	-30	25 -180	mV mA
Oscillator Section 6/				
Initial Accuracy	$T_J = 25^{\circ}\text{C}$	47	57	KHz
Voltage Stability	$V_{IN} = 12\text{V}$ to 25V		1	%
Temperature Stability 1/	Over Operating Range		TBD	%
Amplitude	$V_{RT/CT}$ (peak to peak)		TBD	V
Discharge Current	$T_J = 25^{\circ}\text{C}$ Over Operating Range	7.8 7.0	8.8 9.0	mA mA
Error Amp Section				
Input Voltage, V_{FB}	$V_{COMP} = 2.5\text{V}$	2.45	2.55	V
Input Bias Current, I_{IB}	$2\text{V} \leq V_o \leq 4\text{V}$		-1	μA
Open Loop Gain, A_{VOL}		65		dB
Unity Gain Bandwidth 1/	$T_J = 25^{\circ}\text{C}$	0.7		MHz
PSRR	$12\text{V} \leq V_{CC} \leq 25\text{V}$	60		dB
Output Sink Current	$V_{FB} = 2.7\text{V}$,	2		mA
	$V_{COMP} = 1.1\text{V}$			
Output Source Current	$V_{FB} = 2.3\text{V}$,	-0.5		mA
	$V_{COMP} = 5\text{V}$			
High Level Output Voltage	$V_{FB} = 2.3\text{V}$, $R_L = 15\text{K}$ to gnd	5		V
Low Level Output Voltage	$V_{FB} = 2.7\text{V}$, $R_L = 15\text{K}$ to V_{REF}		1.1	V
Current Sense Section				
Gain 2/ 3/		2.85	3.15	V/V
Maximum Input Signal 2/	$V_{COMP} = 5\text{V}$.9	1.1	V
PSRR 3/	$12\text{V} \leq V_{CC} \leq 25\text{V}$	TBD		dB
Input Bias Current			-10	μA
Delay to Outputs 1/			300	ns
PWM Section				
Max. Duty Cycle		93	100	%
Min. Duty Cycle			0	%

Output Section				
Output Low Level	$I_{SINK} = 20\text{mA}$ $I_{SINK} = 200\text{mA}$		0.4 2.2	V V
Output High Level	$I_{SOURCE} = 20\text{mA}$ $I_{SOURCE} = 200\text{mA}$	13 12		V V
Rise Time 1/ Fall Time 1/	$C_L = 1\text{nF}, T_J = 25^\circ\text{C}$ $C_L = 1\text{nF}, T_J = 25^\circ\text{C}$		150 150	ns ns
Under-Voltage Lockout Section				
Start-Up Threshold		15	17	V
Min. Operating Voltage	After Turn On	9	11	V
Power Consumption Section				
Start-up Current			1	mA
Operating Supply Current ICC	$V_{FB} = V_{ISENSE} = 0\text{V}$		17	mA
V_{CC} Zener Voltage	$I_{CC} = 25\text{mA}$		TBD	V

NOTES: 1/ These parameters, although guaranteed, are not 100% tested in production.

2/ Parameter measured at trip point of latch with $V_{FB} = 0$.

3/ Gain defined as: $G = (\Delta V_{COMP}) / (\Delta V_{ISENSE})$; $0 \leq V_{ISENSE} \leq 0.8\text{V}$.

4/ Adjust V_{CC} above the start threshold before setting at 15V.

Table VI. Delta Limits for SG1524B, SG1526B, SG1842 and SG1846 at $T_A=25^\circ\text{C}$

PARAMETERS	DELTA LIMITS
I_{CC}	$\pm 10\%$ of initial reading
I_{CEX}	$\pm 10\%$ of initial reading or $\pm 2\mu\text{A}$ W.I.G.
I_{IB}	$\pm 10\%$ of spec. limit
V_{REF}	$\pm 50\text{mV}$
V_{IO}	$\pm 1\text{mV}$

Table VII. SG1532 Electrical Characteristics
Unless otherwise specified, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{IN}=10\text{V}$, $V_{OUT}=5\text{V}$
and $I_{OUT}=1\text{mA}$.

Parameter	Test Conditions	Spec.Limit		Units
		MIN	MAX	
Input Voltage Range	$T_A = 25^\circ\text{C}$	4.5	50	V
Input Voltage Range	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.7	50	V
Output Voltage Range	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.0	38	V
Output Current	$R_{SC}=0$, $V_{OUT}=0$, $T_A=25^\circ\text{C}$		250	mA
Min($V_{IN}-V_{OUT}$)	$I_{OUT}=100\text{mA}$, $T_A=25^\circ\text{C}$		2.0	V
Reference Voltage	$T_A=25^\circ\text{C}$	2.40	2.60	V
Reference Voltage	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.35	2.65	V
Temperature Stability	2/		.015	%/ $^\circ\text{C}$
Reference Short Circuit Current	$V_{REF}=0$, $T_A=25^\circ\text{C}$		25	mA
Line Regulation 1/	$8\text{V} \leq V_{IN} \leq 40\text{V}$		0.01	%/V
Line Regulation 1/	$8\text{V} \leq V_{IN} \leq 20\text{V}$, $I_{OUT}=25\text{mA}$		0.02	%/V
Load Regulation 1/	$1\text{mA} \leq I_{OUT} \leq 25\text{mA}$.004	%/mA
Load Regulation 1/	$1\text{mA} \leq I_{OUT} \leq 100\text{mA}$.005	%/mA
Current Limit Sense Voltage	$R_{SC}=100\text{ohm}$, $V_{OUT}=0\text{V}$	0.06	0.10	V
Shutdown Voltage Threshold		0.4	1.0	V
Shutdown Source Current	$V_{OUT}=\text{high}$	100	300	μA
Zener Voltage	$I_{OUT}=10\text{mA}$	6.0	7.2	V
Standby Current	$V_{IN}=40\text{V}$		3.5	mA
Error Amplifier Offset Voltage			10	mV
Error Amplifier Input Bias Current			15	μA
Open Loop Gain	$T_A=25^\circ\text{C}$	66		dB

NOTES:

1/ Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

2/ These parameters are guaranteed over the recommended operating conditions.

Table VIII. Delta Limits for SG1532 at $T_A=25^\circ C$

Parameters	Delta Limits
V_{REF}	$\pm 50 \text{ mV}$
$I_{STANDBY}$	$\pm 10\%$
V_{IO}	$\pm 1 \text{ mV}$
I_{IB}	$\pm 10\% \text{ or } \pm 0.5 \mu\text{A}$, whichever is greater
$V_{IN} - V_{OUT}$	$\pm 10\%$

Table IX. SG1644 Electrical Characteristics
Unless otherwise specified, $-55^\circ C \leq T_A \leq +125^\circ C$ and $V_{CC}=20V$.

Parameter	Test Conditions	Spec. Limit		Units
		MIN	MAX	
Static Characteristics, $-55^\circ C < T_A < +125^\circ C$				
Logic 1 Input Voltage		2.0		V
Logic 0 Input Voltage			0.7	V
Input High Current, I_{IH1}	$V_{IN}=2.4V$		400	μA
Input High Current, I_{IH2}	$V_{IN}=5.5V$		1.0	mA
Input Low Current, I_{IL}	$V_{IN}=0V$		-4.0	mA
Input Clamp Voltage	$I_{IN}=-10\text{mA}$		-1.5	V
Output High Voltage, I_1	$I_{OUT}=-200\text{mA}$	$V_{CC}-3$		V
Output Low Voltage, I_1	$I_{OUT}=200\text{mA}$		1.0	V
Supply Current Outputs Low, I_{CCL}	$V_{IN}=0V$ (both inputs)		27	mA
Supply Current Outputs High, I_{CCH}	$V_{IN}=2.4V$ (both inputs)		12	mA
Dynamic Characteristics 3/, $T_A=25^\circ C$				
Propagation Delay, High-to-Low	$C_L=1000\text{pF}$ 2/ $C_L=2500\text{pF}$		30 35	ns
Propagation Delay, Low-to-High	$C_L=1000\text{pF}$ 2/ $C_L=2500\text{pF}$		25 30	ns
Rise Time (TTLH)	$C_L=1000\text{pF}$ 2/ $C_L=2500\text{pF}$		30 40	ns

Fall Time (TTHL)	$C_L=1000\text{pF}$ <u>2/</u> $C_L=2500\text{pF}$		25 40	ns
Supply Current (I_{cc})	$C_L=2500\text{pF}$, $f=200\text{KHz}$, Duty Cycle=50%		35	mA
Dynamic Characteristics, 3/, $-55^\circ\text{C} < T_A < +125^\circ\text{C}$				
Propagation Delay High-to-Low	$C_L=1000\text{pF}$ <u>2/</u> $C_L=2500\text{pF}$		40 50	ns
Propagation Delay Low-to-High	$C_L=1000\text{pF}$ <u>2/</u> $C_L=2500\text{pF}$		30 40	ns
Rise Time (TTLH)	$C_L=1000\text{pF}$ <u>2/</u> $C_L=2500\text{pF}$		35 50	ns
Fall Time (TTHL)	$C_L=1000\text{pF}$ <u>2/</u> $C_L=2500\text{pF}$		30 50	ns
Supply Current (I_{cc})	$C_L=2500\text{pF}$, $f=200\text{KHz}$, Duty Cycle=50%		40	mA

Notes: 1/ $V_{cc}=10\text{V}$ to 20V .

2/ These parameters, specified at 1000pF , although guaranteed over recommended operating conditions, are not tested in production.

3/ $V_{cc}=15\text{V}$.

4/ Pulsed. Pulse width $\leq 500\text{ ns}$; duty cycle $\leq 1\%$.

Table X. Delta Limits for SG1644 at $T_A=25^\circ\text{C}$

Parameter	Delta Limit
$I_{\text{CCL}}, I_{\text{CCH}}, I_{\text{IL}}$	$\pm 10\%$
$I_{\text{IH1}}, I_{\text{IH2}}$	$\pm 10\%$ or one microampere, whichever is greater.
TTLH, TTHL	$\pm 20\%$

Figure 1. SG1526B Connection Diagram (18-pin DIP)

Figure 2. SG1526B Connection Diagram (24-lead Flatpack)

Figure 3. SG1526B Connection Diagram (20-lead Flatpack)

Figure 4. SG1524B Connection Diagram (16-pin DIP)

Figure 5. SG1524B Connection Diagram (16-lead Flatpack)

Figure 6. SG1846 Connection Diagram (16-pin DIP)

Figure 7. SG1846 Connection Diagram (16-lead Flatpack)

Figure 8. SG1842 Connection Diagram (10-lead Flatpack)

Figure 9. SG1526B Block Diagram

Figure 10. SG1524B Block Diagram

Figure 11. SG1846 Block Diagram

Figure 12. SG1842 Block Diagram

Figure 13. SG1526B Static Burn-in Circuit

Figure 14. SG1526B Dynamic Burn-in Circuit

Figure 15. SG1524B Static Burn-in Circuit

Figure 16. SG1524B Dynamic Burn-in Circuit

Figure 17. SG1846 Static Burn-in Circuit

Figure 18. SG1846 Dynamic Burn-in Circuit

Figure 19. SG1532 Connection Diagram (14-Lead Flatpack)

FIGURE 20. SG1644 Connection Diagram 14-Lead, D.I.P

FIGURE 21. SG1532 Block Diagram

Figure 22. SG1644 Equivalent Circuit Schematic

Figure 23. SG1532 Burn-in Circuit and Life Test Circuit

Figure 24. SG1644 Static Burn-in Circuit

Figure 25. SG1644 Dynamic Burn-in Circuit and Life Test Circuit

Figure 26. SG1842 Static Burn-in Circuit.

Figure 27. SG1842 Dynamic Burn-in Circuit

Figure 28. SG1644 Connection Diagram, 10 Lead Flat Pack